EFFECTIVE POWER AND GROUND DISTRIBUTION SCHEME FORDEEP SUBMICRION HIGH SPEED VLSI CIRCUITS

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ABSTRACT

This paper studies the power and ground distribution and its noise effect for deep submicron CMOS VLSI circuits. It is found that orders of magnitude reduction in switching noise can be achieved using an effective power and ground distribution scheme introduced in this paper.

1. INTRUDUCTION

In the early days of VLSI, the design of power distribution for an integrated circuits was rather simple. Lower speeds and circuit density made the choice of the wire width easier: just made them fat enough to avoid resistive voltage drop due to switching currents in the power supply. Later synthesis tools have considered simplified DC, AC and transient interaction aspects which improve the design by optimizing the power I/O cell assignment, the power bus topology selection, and the power bus sizing via simulated annealing algorithms [1]. Nonetheless, the existing power synthesis algorithms are still inadequate when the technology is moved deeper into submicron generations (0.18~0.05 μm generations). The increased clock speed and huge integration density will result in a power dissipation approaching to 20W/cm^2 for instance in future microprocessors [2], which correlates a reasonable power density limit for an air-cooled package device. Such a power density is equivalent to an average current of 16.67A for 1.2V supply in 0.1μm CMOS. Assume that the current is uniformly distributed with an Al-Cu sheet of 1μm thick, the average current density is thus as high as 1.67mA/μm^2. Such a high current density causes 0.367V/cm DC voltage drop on Al-Cu wires (ρ=2.2μΩcm) and also perhaps some reliability concerns such as electromigration. Multiple power planes may thus be utilized which allows more flexibility in the topological layout of the power networks. Moreover, when the internal clock runs at GHz, fast switching rise time causes a huge simultaneous switching current which results in a substantial switching noise (*i.e.* ΔI noise) and ground bounce in the supply network. On-chip decoupling capacitors are thus required to reduce this switching noise. Early works use such as metal-insulator-metal capacitors on the top of the chip, or use large MOS transistor capacitors etc. [3-5]. Whereas, in deep submicron VLSI circuits, different functional metallization layers may be available [6-7]. This provides a new degree of freedom in design floorplans and geometric topology of power network. We so far can use the decoupling effect of the interconnect parasitic capacitors through the power network itself.

In this paper, we address an effective on-chip power and ground distribution scheme for deep submicron high speed VLSI circuits. By incorporating the complex LRC parasitic and on-chip decoupling effect of the power network, noise on power/ground nets is studied for various power bus topology and sizing. We show that when VLSI circuits clock at very high speed, orders of magnitude reduce in switching noise can be achieved by slicing the power/ground planes and/or wide on-chip power/ground wires into multiple small wires with power and ground evenly distributed. High aspect ratio wire (height: width ratio) with short separation between V_{DD} and GND are hence a promising wire geometry for low noise power network.

2. NOISE ON A DISTRIBUTED POWER LINE

To feed such larger power dissipation, one possible way is to deposit very thick metal layers on the top of the chip as power and ground planes. The distance between the load and the power and ground planes thus becomes shorter and hence the voltage drop on the wires is reduced. An alternative way is to insert multiple power and ground planes between signal layers, as the style which is used in today's multi-layer print circuits board designs. This method also provides better signal isolation. The drawback is increasing the number of interconnect layers and signal layer to signal layer connecting. And the third possibility is to use two stacked metal layers (separated by the dielectrics) for ground and power respectively instead of distributing power and ground on the same metal layers. Of course one need to do more vias through one of the layers, which is a drawback. Additionally, thermal mismatch between metal and dielectrics would yield some manufacture problems for such a structure.

No matter which style is used, there is less trick we can do to decrease this dc voltage drop other than increasing the total

cross section of wires and decreasing the distance between power pin and the load. However, for ΔI noise, we can control it by optimizing the interconnect geometry and technology process.

If we only consider the on-chip power distribution, the ΔI noise on a power line is:

$$V_{\Delta i} = L\frac{di_L}{dt} \qquad (1)$$

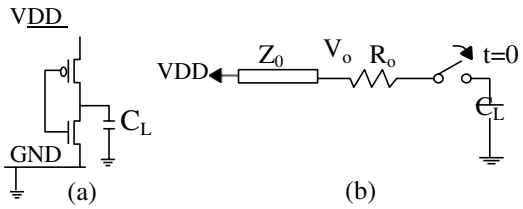

Figure 1. An illustration of an on-chip power line drive a CMOS load capacitor (a) and its simplified equivalent circuit (b).

where L is the parasitic inductance of the power line, i_L is switching current on that power line. However, it should be mentioned that for on-chip wires, the power and ground lines are LC distributed lines rather than a simple inductance. An equivalent circuit for an on-chip power wire driving a load capacitance is shown in Fig.1,where Z_0 is the characteristic impedance of this LC distributed line and R_o is the dynamic output resistance of the gate. C_L is the load capacitance.

Assume that V_{DD} is well terminated and there is no reflection, the maximum voltage drop at V_o for a voltage swing of ΔV on C_L is then:

$$V_{\Delta i} \approx \frac{\Delta V Z_0}{R_0 + Z_0} = \frac{0.8 V_{DD} Z_0 C_L}{2.2 t_r} \qquad (2)$$

where t_r is the output signal rise time which is defined between 10% and 90% of the total output voltage swing.

For a specific load capacitance and switching rise time, Eq.(2) indicates that the switching noise is proportional to the characteristic impedance of the power line. Therefore, to reduce ΔI noise on power and ground lines, one need to design these lines as low impedance wires. Parasitic inductance and characteristic impedance of interconnect wires with various geometries are shown in Fig.2. The inductance shown in the figure is the total parasitic inductance which includes self and

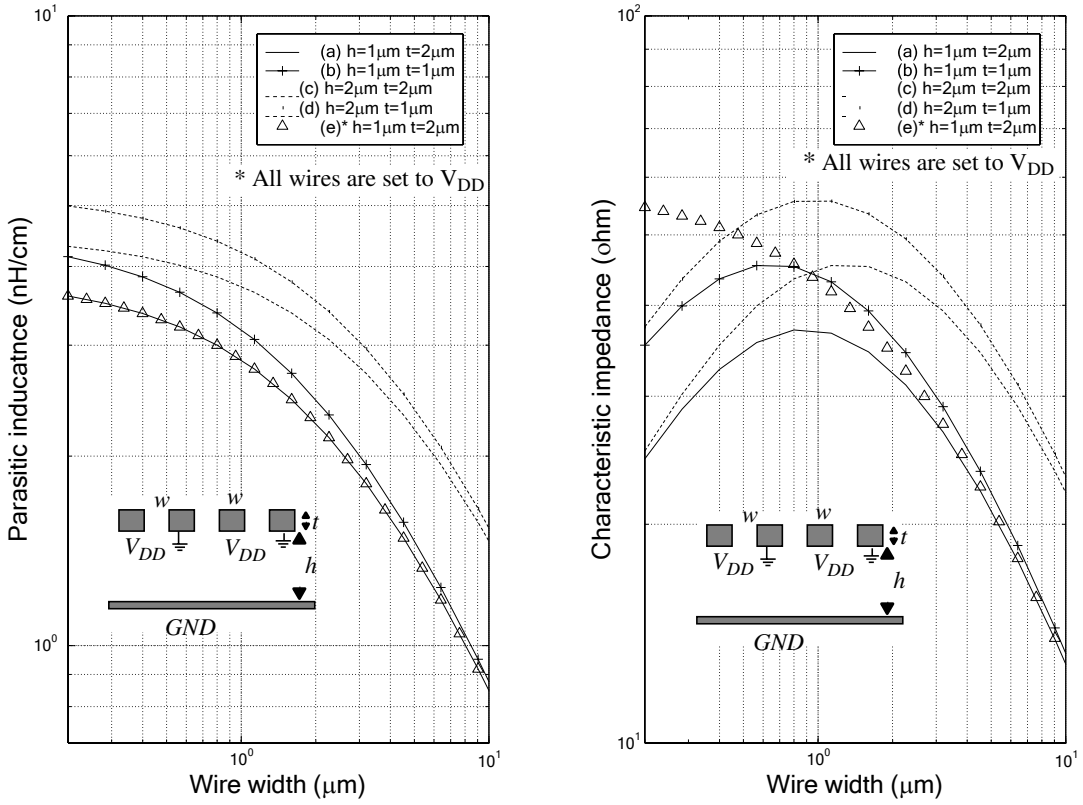

Figure 2. Dependence of parasitic inductance and characteristic impedance of a distributed power line on its width. The power distribution is shown in the insert of the figures. The geometry of the wire is shown in the legend of the figures. Curves (e) are the case that all wires in the top layer are set to V_{DD}, so the mutual capacitance between two neighbour wires is zero.

inductances. They are computed by re-computing the capacitance matrix $\boldsymbol{C_0}$ of self and mutual capacitance matrix for the same conductor in a free space using the following simple relationship:

$$\boldsymbol{LC_0}=\varepsilon_0\mu_0\boldsymbol{I} \quad (3)$$

with $\boldsymbol{I}$ the unit matrix, $\boldsymbol{C_0}$ a 2-dimensional capacitance matrix (*i.e.* per unit length capacitance matrix) in this work.

For an evenly distributed power network shown in the insert of Fig.2, the parasitic inductance increases when the wire width decreases. However, this is not the case for characteristic impedance. The characteristic impedance decreases when the wire width is less than 1μm. This is due to the contribution of mutual capacitance between the power line and the neighbour ground wires. If we set all of the wires to V_{DD}, as curve (e) in Fig.2 shows, the characteristic impedance increases monotonously when the wire width decreases (because the mutual capacitance between two neighbour wires is zero in this case).

The decrease in ΔI noise for low impedance power lines can be simply interpreted as the effect of using decoupling capacitor, because low impedance means low *L* and/or large *C*, the first one induces low noise according to Eq.(1) while later one acts as a large on-chip decoupling capacitor. Therefore, in power distribution design, it is always important to place the power and ground wires as close as possible.

3. NOISE ON A DISTRIBUTED POWER NETWORK AND ITS OPTIMUM SCHEME

The above analysis is only for routing a single or small amount of power lines. It will be more interesting to distribute the power and ground planes. Consider an evenly distributed power and ground network with a plane of 1cm by *l* cm as shown in Fig.3. Total number of *N* power/ground pairs drive a total load capacitance of C_L. The ΔI noise is then given by:

$$V_{\Delta i} \approx \frac{0.8V_{DD}Z_0C_L}{2.2Nt_r} = \frac{0.8V_{DD}Z_pC_L}{2.2t_r} \quad (4)$$

with Z_p the total impedance of power lines which is equal to Z_0/N. Suppose the power and ground lines have the same geometry and the separation *d* between the neighbour wires is also *w* (the wire width), so the number of power lines across 1cm is $N=1/4w$ (we call it the power wire density hereafter).

The total inductance and characteristic impedance as a function power wire density is shown in Fig.4. It is found that slicing a wide wire into many narrow wires with high aspect ratio can decrease the switching noise order of magnitude. Consider for instance a 0.1μm CMOS chip with an average load capacitance of 2.5fF/gate and signal rise time of 200psec. If there are 20% gates being switched simultaneously, the total load capacitance for a 6M gates/cm^2 design is 3nF. To drive such a big load, one uses a power plane with total 1,000 power lines (h=6μm, t=1μm, and each wire width is 2.5μm, so the total power plane width is 1cm). The switching noise then

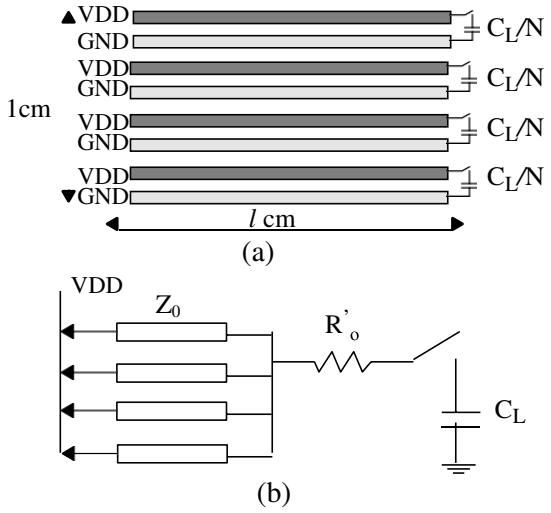

Figure 3. An illustration of power distribution (a) and its simplified equivalent circuit (b) for analysing the efficiency of power planes.

equals 0.49V for a 1.2V supply. If we slice the wires into a width of 0.25μm for each (so total have 10,000 power lines, and the power plane width is still 1cm), the switching noise then equals 23mV, 20 times improvement! It should be noted that the value of dc voltage drop are the same for both cases in this example.

If we set all wires of top layer at V_{DD}, the resulting inductance and characteristic impedance are shown as curves (f) and (g) in Fig.4. It is found that this may give larger switch noise than that when V_{DD} and *GND* run parallel to each other in a power plane.

4. SUMMARY

We have studied various on-chip power/ground distributions and its noise effect. It is found that placing power and ground wires one-by-one evenly on the same plane can decrease impedance considerably and thereby reduce switching noise. This distribution is better than the two stacked metal style where one is as power plane and another is as ground plane. The reason is that this distribution gives larger parasitic capacitance due to the fringing and interwire capacitance which acts as on-chip decoupling capacitance. According to this understand, we have sliced wide power/ground wires or planes

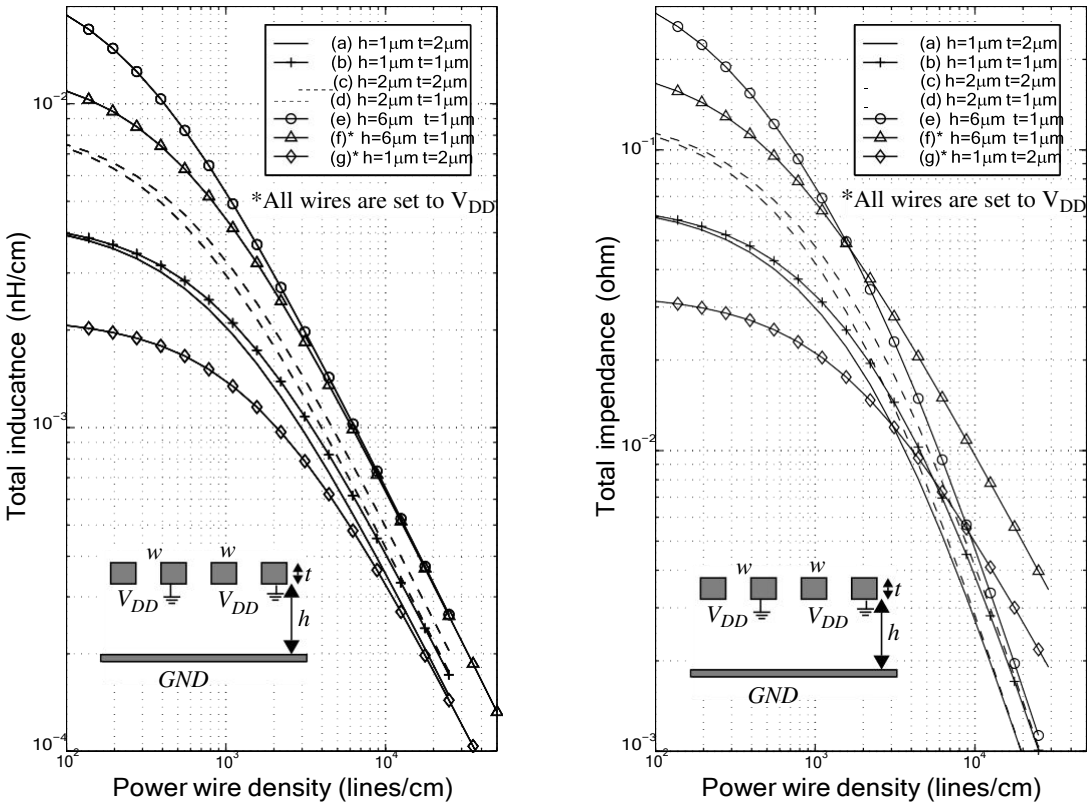

Figure 4. Dependence of parallel inductance and parallel characteristic impedance of total power lines over 1cm width on the power wire density. The distribution of the lines are shown in the inserts of the figure where all wires have the same width *w* and the pitch width is 2*w*. Curves (f) and (g) are the case that all wires in the top layer are set to V_{DD}.

into many high aspect ratio small wires, and setting them to V_{DD} and GND one by one evenly. Both of them have the same DC voltage drop but the later one has given much lower switching noise. Additionally, the power lines should always run as close as possible to the ground lines to minimize the enclosed area and hence minimize parasitic inductance and increase on-chip capacitance decoupling. We see that such an effective power distribution will not meet a manufacture problem in deep submicron generations because of the improvements in technology particularly the application of dual damascene process in interconnect fabrication. The utilization of high thickness:width aspect ratio interconnect wires and high dielectric constant films in advanced integrated circuits offers a good opportunity for such a power and ground distribution.

5. REFERENCES

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